**Amendments to the Claims:**

This listing of claims will replace all prior versions, and listings, of claims in the application:

**Listing of Claims**

1. (Currently Amended) An image processor comprising an image processing circuit image-processing image data input therein and a main memory receiving and temporarily storing transferred said data processed in said image processing circuit, wherein

said image processing circuit has a temporary storage area temporarily storing pixel data of a plurality of lines of said image data, image dividing means dividing said image data into divided image data storable in said temporary storage area, single pixel processing means executing image processing on said divided image data in units of single pixels and multiple pixel processing means executing image processing in units of multiple pixels after said temporary storage area stores said divided image data processed in said single pixel processing means, thus creating processed divided image data, and

said main memory has a first buffer area storing first processed divided image data continuously processed in said single pixel processing means and said multiple pixel processing means among said divided image data, a second buffer area storing second processed divided image data processed in said single pixel processing means among said divided image data and a third buffer area storing data obtained by processing said second processed divided image data read from said second buffer area in said multiple pixel processing means,

said image processor further comprising image combining means combining said first processed divided image data stored in said first buffer area and said data stored in said third buffer area with each other.

2. (Original) The image processor according to claim 1, wherein a CPU (central processing unit) controls data transfer between said main memory and said image processing circuit.

3. (Original) The image processor according to claim 1, further comprising a DMA (direct memory access) controller controlling data transfer between said main memory and said image processing circuit.

4. (Original) The image processor according to claim 3, wherein said DMA controller has at least two DMA channels, first said DMA channel is assigned to data transfer from said multiple pixel processing means to said first buffer area and second said DMA channel is assigned to data transfer from said single pixel processing means to said second buffer area.

5. (Original) The image processor according to claim 3, wherein said DMA controller has at least two DMA channels, first said DMA channel is assigned to data transfer from said second buffer area to said multiple pixel processing means and second said DMA channel is assigned to data transfer from said multiple pixel processing means to said third buffer area.

6. (Currently Amended) An image processor comprising an image processing circuit image-processing image data input therein, a main memory receiving and temporarily storing transferred said data processed in said image processing circuit and a DMA controller controlling data transfer between said main memory and said image processing circuit, wherein

said image processing circuit has a temporary storage area temporarily storing pixel data of a plurality of lines of said raw image data, image dividing means dividing said image data into divided image data storable in said temporary storage area, single pixel processing means executing image processing on said divided image data in units of single pixels and multiple pixel processing means executing image processing in units of multiple pixels after said temporary storage area stores said divided image data processed in said single pixel processing means, thus creating processed divided image data,

said main memory has a first buffer area storing first processed divided image data continuously processed in said single pixel processing means and said multiple pixel processing means among said divided image data and a second buffer area storing second processed divided image data processed in said single pixel processing means among said divided image data,

said first buffer area also stores data obtained by processing said second processed divided image data read from said second buffer area in said multiple pixel processing means, and

said DMA controller makes addressing when transferring said first and second processed divided image data to said first buffer area thereby combining the same into a single image and storing said single image.

7. (Original) The image processor according to claim 6, wherein said DMA controller comprises a DMA channel generating and outputting an address on said main memory and a memory control circuit executing data transfer between a storage element corresponding to said address output from said DMA channel and said image processing circuit, and

said DMA channel comprises:

an address counter generating and outputting said address by sequentially changing the same from a prescribed start address in said first buffer area up to a prescribed end address in said first buffer area,

a local counter performing counting in synchronization with sequential change of said address in said address counter, and

an adder-subtracter outputting an added/subtracted value obtained by adding/subtracting a prescribed offset value to/from said address output from said address counter when a count output from said local counter reaches a prescribed final value to said address counter thereby making said address counter change said address from said added/subtracted value.